REMARKS

Claims 1, 2, 3, 7, 8, 9, 11, 12 and 13 have been amended to clarify the invention and overcome the Examiner's rejections.

Pursuant to 37 CFR § 1.121, a marked copy of the amended claims showing the changes made therein accompanies this Amendment. No new matter has been entered.

Turning to the rejections under 35 USC § 112, claims 11-13 have been amended to change "side walls" to "side wall" in order to overcome the Examiner's indefiniteness rejection for lack of antecedent basis for the term "side walls." Thus, Applicant respectfully submits the Examiner's rejection has been rendered moot.

Turning to the rejection of claims 1, 3, 4, 6, 11, 13, 14 and 16 under 35 USC § 103 as obvious over U.S. Patent 6,018,170 to Gardner et al., claims 1 and 3 have been amended to specify that the "side wall [is] formed on the surface of said gate electrode so as to be covered behind a visor portion. . . as seen in plan view." Gardner et al. teaches a side wall that is covered by the electrode when seen in plan view, but fails to teach an electrode with a visor portion (Figures 1, 2, 3, 4 and 5). Since claims 1 and 3 require an electrode with a visor portion, Gardner et al. is missing an entire element, and cannot render obvious the instant claims and all claims dependent therefrom.

The Examiner further rejects claims 2, 5, 10, 12 and 15 under 35 USC § 103 as obvious over Gardner et al. in view of U.S. Patent 6,204,538 to Kim. Claim 2 has been amended to specify that the "side wall [is] formed on the surface of said gate electrode so as to be covered behind a visor portion . . . as seen in plan view." As discussed in the previous paragraph, Gardner et al. does not teach this element. Kim also fails teach an electrode with a visor portion

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(Figures 4b and 4c). Thus, no combination of Gardner et al. and Kim would achieve claim 2 or the several claims dependent thereon.

Having dealt with all of the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on October 16, 2002, at Tucson, Arizona.

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MARKED COPY OF AMENDED CLAIMS

SERIAL NO. 10/036,955

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MARKED CLAIMS SHOWING CHANGES MADE

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a [top part] visor portion of said gate electrode as seen in plan view; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall.

2. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a [top part] visor portion of said gate electrode as seen in plan view;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall.

3. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a [top part] visor portion of said gate electrode as seen in plan view, said side wall being formed of a lamination of at least two insulation films having different etching properties.

7. (Amended) The semiconductor device according to claim 4, wherein [said gate electrode further comprises a visor part on said upper part] the width of said visor portion is substantially constant and [the greatest] greater in [the] length along said gate length direction than said upper or lower parts.

8. (Amended) The semiconductor device according to claim 5, wherein [said gate electrode further comprises a visor part on said upper part] the width of said visor portion is substantially constant and [the greatest] greater in [the] length along said gate length direction than said upper or lower parts.

9. (Amended) The semiconductor device according to claim 6, wherein [said gate electrode further comprises a visor part on said upper part] the width of said visor portion is substantially constant and [the greatest] greater in [the] length along said gate length direction than said upper or lower parts.

11. (Amended) The semiconductor device according to claim 4, wherein said side [walls are] wall is formed on both a side surface of said upper part and [on] a side surface of said lower part and is formed out of at least two different insulation films[, respectively].

12. (Amended) The semiconductor device according to claim 5, wherein said side [walls are] wall is formed on both a side surface of said upper part and [on] a side surface of said lower part and is formed out of at least two different insulation films[, respectively].

13. (Amended) The semiconductor device according to claim 6, wherein said side [walls are] wall is formed on both a side surface of said upper part and [on] a side surface of said lower part and is formed out of at least two different insulation films[, respectively].